The LTC®2498 is a 16-channel (8-differential) 24-bit No Latency ΔΣ™ ADC with Easy Drive technology. The patented sampling scheme eliminates dynamic input current errors and the shortcomings of on-chip buffering through automatic cancellation of differential input current. This allows large external source impedances, and rail-to-rail input signals to be directly digitized while maintaining exceptional DC accuracy.

The LTC2498 includes a high accuracy temperature sensor and an integrated oscillator. This device can be configured to measure an external signal (from combinations of 16 analog input channels operating in single ended or differential modes) or its internal temperature sensor. The integrated temperature sensor offers 1/30th °C resolution and 2°C absolute accuracy.

The LTC2498 allows a wide common mode input range (0V to VCC), independent of the reference voltage. Any combination of single-ended or differential inputs can be selected and the first conversion after a new channel is selected is valid. Access to the multiplexer output enables optional external amplifiers to be shared between all analog inputs and auto calibration continuously removes their associated offset and drift.
**LTC2498**

**ABSOLUTE MAXIMUM RATINGS**

(Notes 1, 2)

Supply Voltage (VCC) ................................... –0.3V to 6V
Analog Input Voltage
(CH0 to CH15, COM) ..................................–0.3V to (VCC + 0.3V)
Reference Input Voltage
ADCINN, ADCINP, MUXOUTP, MUXOUTN ................–0.3V to (VCC + 0.3V)
Digital Input Voltage ................................. –0.3V to (VCC + 0.3V)
Digital Output Voltage .................................–0.3V to (VCC + 0.3V)
Operating Temperature Range
LTC2498C ................................................ 0°C to 70°C
LTC2498I .............................................–40°C to 85°C
LTC2498H .......................................... –40°C to 125°C
Storage Temperature Range .......................–65°C to 150°C

**PARAMETER CONDITIONS MIN TYP MAX UNITS**

Resolution (No Missing Codes) 0.1V ≤ V REF ≤ VCC, –FS ≤ VIN ≤ +FS (Note 5) 24 Bits
Integral Nonlinearity 5V ≤ VCC ≤ 5.5V, VREF = 5V, VIN(CM) = 2.5V (Note 6)
H Grade 2.7V ≤ VCC ≤ 5.5V, VREF = 2.5V, VIN(CM) = 1.25V (Note 6) ● 2 10 ppm of VREF ● 1 ppm of VREF
Offset Error 2.5V ≤ VREF ≤ VCC, GND ≤ IN+ = IN– ≤ VCC (Note 14) ● 0.5 2.5 µV
Offset Error Drift 2.5V ≤ VREF ≤ VCC, GND ≤ IN+ = IN– ≤ VCC 10 nV/°C
Positive Full-Scale Error 2.5V ≤ VREF ≤ VCC, IN+ = 0.75VREF, IN– = 0.25VREF ● 25 ppm of VREF
Positive Full-Scale Error Drift 2.5V ≤ VREF ≤ VCC, IN+ = 0.75VREF, IN– = 0.25VREF 0.1 ppm of VREF/°C
Negative Full-Scale Error 2.5V ≤ VREF ≤ VCC, IN+ = 0.25VREF, IN– = 0.75VREF ● 25 ppm of VREF
Negative Full-Scale Error Drift 2.5V ≤ VREF ≤ VCC, IN+ = 0.25VREF, IN– = 0.75VREF 0.1 ppm of VREF/°C

**ORDER INFORMATION**

LEAD FREE FINISH TAPE AND REEL PART MARKING* PACKAGE DESCRIPTION TEMPERATURE RANGE
LTC2498CUHF#PBF LTC2498CUHF#TRPBF 2498 38-Lead (5mm × 7mm) Plastic QFN 0°C to 70°C
LTC2498IUHF#PBF LTC2498IUHF#TRPBF 2498 38-Lead (5mm × 7mm) Plastic QFN –40°C to 85°C
LTC2498HUHF#PBF LTC2498HUHF#TRPBF 2498 38-Lead (5mm × 7mm) Plastic QFN –40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. * The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

**ELECTRICAL CHARACTERISTICS (NORMAL SPEED)**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. (Notes 3, 4)
## LTC2498

### Electrical Characteristics (Normal Speed)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. (Notes 3, 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution (No Missing Codes)</td>
<td>0.1V ≤ V_REF ≤ V_CC, –FS ≤ V_IN ≤ +FS (Note 5)</td>
<td>24</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Integral Nonlinearity</td>
<td>2.5V ≤ V_CC ≤ 5.5V, V_REF = 5V, V_IN(CM) = 2.5V (Note 6)</td>
<td>●</td>
<td>2</td>
<td>10</td>
<td>ppm of V_REF</td>
</tr>
<tr>
<td>Offset Error</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = IN– = IN+ ≤ IN– = V_CC (Note 14)</td>
<td>●</td>
<td>0.5</td>
<td>2</td>
<td>mV</td>
</tr>
<tr>
<td>Offset Error Drift</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = IN– = IN+ ≤ IN– = V_CC (Note 14)</td>
<td></td>
<td>100</td>
<td></td>
<td>nV/°C</td>
</tr>
<tr>
<td>Positive Full-Scale Error</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = 0.75V_REF, IN– = 0.25V_REF (Note 16)</td>
<td>●</td>
<td></td>
<td>25</td>
<td>ppm of V_REF</td>
</tr>
<tr>
<td>Positive Full-Scale Error Drift</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = 0.75V_REF, IN– = 0.25V_REF (Note 16)</td>
<td></td>
<td></td>
<td>0.1</td>
<td>ppm of V_REF°C</td>
</tr>
<tr>
<td>Negative Full-Scale Error</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = 0.25V_REF, IN– = 0.75V_REF (Note 16)</td>
<td>●</td>
<td></td>
<td>25</td>
<td>ppm of V_REF</td>
</tr>
<tr>
<td>Negative Full-Scale Error Drift</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = 0.25V_REF, IN– = 0.75V_REF (Note 16)</td>
<td></td>
<td></td>
<td>0.1</td>
<td>ppm of V_REF°C</td>
</tr>
<tr>
<td>Output Noise</td>
<td>5V ≤ V_CC ≤ 2.5V, V_REF = 5V, GND ≤ IN+ = IN– ≤ V_CC</td>
<td></td>
<td></td>
<td>0.85</td>
<td>µV RMS</td>
</tr>
</tbody>
</table>

### Electrical Characteristics (2x Speed)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. (Notes 3, 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution (No Missing Codes)</td>
<td>5V ≤ V_CC ≤ 5.5V, V_REF = 2.5V, V_IN(CM) = 1.25V (Note 5)</td>
<td></td>
<td>24</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Integral Nonlinearity</td>
<td>5V ≤ V_CC ≤ 5.5V, V_REF = 5V, V_IN(CM) = 2.5V (Note 6)</td>
<td>●</td>
<td>2</td>
<td>10</td>
<td>ppm of V_REF</td>
</tr>
<tr>
<td>Offset Error</td>
<td>2.7V ≤ V_CC ≤ 5.5V, V_REF = 2.5V, V_IN(CM) = 1.25V (Note 6)</td>
<td>●</td>
<td>0.5</td>
<td>2</td>
<td>mV</td>
</tr>
<tr>
<td>Offset Error Drift</td>
<td>2.7V ≤ V_CC ≤ 5.5V, V_REF = 2.5V, V_IN(CM) = 1.25V (Note 6)</td>
<td></td>
<td>100</td>
<td></td>
<td>nV/°C</td>
</tr>
<tr>
<td>Positive Full-Scale Error</td>
<td>5V ≤ V_REF ≤ V_CC, IN+ = 0.75V_REF, IN– = 0.25V_REF (Note 16)</td>
<td>●</td>
<td></td>
<td>25</td>
<td>ppm of V_REF</td>
</tr>
<tr>
<td>Positive Full-Scale Error Drift</td>
<td>5V ≤ V_REF ≤ V_CC, IN+ = 0.75V_REF, IN– = 0.25V_REF (Note 16)</td>
<td></td>
<td></td>
<td>0.1</td>
<td>ppm of V_REF°C</td>
</tr>
<tr>
<td>Negative Full-Scale Error</td>
<td>5V ≤ V_REF ≤ V_CC, IN+ = 0.25V_REF, IN– = 0.75V_REF (Note 16)</td>
<td>●</td>
<td></td>
<td>25</td>
<td>ppm of V_REF</td>
</tr>
<tr>
<td>Negative Full-Scale Error Drift</td>
<td>5V ≤ V_REF ≤ V_CC, IN+ = 0.25V_REF, IN– = 0.75V_REF (Note 16)</td>
<td></td>
<td></td>
<td>0.1</td>
<td>ppm of V_REF°C</td>
</tr>
<tr>
<td>Output Noise</td>
<td>5V ≤ V_CC ≤ 2.5V, V_REF = 5V, GND ≤ IN+ = IN– ≤ V_CC</td>
<td></td>
<td></td>
<td>0.85</td>
<td>µV RMS</td>
</tr>
</tbody>
</table>

### Converter Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. (Note 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Common Mode Rejection DC</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = IN– = V_CC (Note 5)</td>
<td>●</td>
<td>140</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input Common Mode Rejection 60Hz ±2%</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = IN– = V_CC (Note 5)</td>
<td>●</td>
<td>140</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input Normal Mode Rejection 50Hz ±2%</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = IN– = V_CC (Note 5)</td>
<td>●</td>
<td>140</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input Normal Mode Rejection 60Hz ±2%</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = IN– = V_CC (Note 5)</td>
<td>●</td>
<td>110</td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td>Input Normal Mode Rejection 50Hz/60Hz ±2%</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = IN– = V_CC (Note 5)</td>
<td>●</td>
<td>87</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Reference Common Mode Rejection DC</td>
<td>2.5V ≤ V_REF ≤ V_CC, IN+ = IN– = V_CC (Note 5)</td>
<td>●</td>
<td>120</td>
<td>140</td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection DC</td>
<td>V_REF = 2.5V, IN+ = IN– = V_CC</td>
<td></td>
<td></td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection, 50Hz ±2%</td>
<td>V_REF = 2.5V, IN+ = IN– = GND (Notes 7, 9)</td>
<td></td>
<td></td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection, 60Hz ±2%</td>
<td>V_REF = 2.5V, IN+ = IN– = GND (Notes 8, 9)</td>
<td></td>
<td></td>
<td>120</td>
<td>dB</td>
</tr>
</tbody>
</table>

### Analog Input and Reference

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN+</td>
<td>Absolute/Common Mode IN+ Voltage (IN+ Corresponds to the Selected Positive Input Channel)</td>
<td>GND – 0.3V V_CC + 0.3V</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IN−</td>
<td>Absolute/Common Mode IN− Voltage (IN− Corresponds to the Selected Negative Input Channel)</td>
<td>GND – 0.3V V_CC + 0.3V</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
**ANALOG INPUT AND REFERENCE**

The ⚫ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input Differential Voltage Range ($IN^+ – IN^-$)</td>
<td>⚫</td>
<td>$-FS$</td>
<td>$+FS$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$FS$</td>
<td>Full Scale of the Differential Input ($IN^+ – IN^-$)</td>
<td>⚫</td>
<td>0.5$V_{REF}$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$LSB$</td>
<td>Least Significant Bit of the Output Code</td>
<td>⚫</td>
<td>$FS/2^{24}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$REF^+$</td>
<td>Absolute/Common Mode $REF^+$ Voltage</td>
<td>⚫</td>
<td>0.1</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$REF^-$</td>
<td>Absolute/Common Mode $REF^-$ Voltage</td>
<td>⚫</td>
<td>GND</td>
<td>$REF^+ – 0.1V$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>Reference Voltage Range ($REF^+ – REF^-$)</td>
<td>⚫</td>
<td>0.1</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$CS(IN^+)$</td>
<td>$IN^+$ Sampling Capacitance</td>
<td></td>
<td>11</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$CS(IN^-)$</td>
<td>$IN^-$ Sampling Capacitance</td>
<td></td>
<td>11</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$CS(V_{REF})$</td>
<td>$V_{REF}$ Sampling Capacitance</td>
<td></td>
<td>11</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DC_LEAK(IN^+)}$</td>
<td>$IN^+$ DC Leakage Current</td>
<td>Sleep Mode, $IN^+ = GND$</td>
<td>−10</td>
<td>1</td>
<td>10</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{DC_LEAK(IN^-)}$</td>
<td>$IN^-$ DC Leakage Current</td>
<td>Sleep Mode, $IN^- = GND$</td>
<td>−10</td>
<td>1</td>
<td>10</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{DC_LEAK(REF^+)}$</td>
<td>$REF^+$ DC Leakage Current</td>
<td>Sleep Mode, $REF^+ = V_{CC}$</td>
<td>−100</td>
<td>1</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{DC_LEAK(REF^-)}$</td>
<td>$REF^-$ DC Leakage Current</td>
<td>Sleep Mode, $REF^- = GND$</td>
<td>−100</td>
<td>1</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$t_{OPEN}$</td>
<td>MUX Break-Before-Make</td>
<td></td>
<td>V$IN \leq 2V_{P_P}$ DC to 1.8MHz</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$QIRR$</td>
<td>MUX Off Isolation</td>
<td></td>
<td></td>
<td>120</td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

**DIGITAL INPUTS AND DIGITAL OUTPUTS**

The ⚫ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>High Level Input Voltage ($CS, fO, SDI$)</td>
<td>2.7$V \leq V_{CC} \leq 5.5V$ (Note 18)</td>
<td>⚫</td>
<td>$V_{CC} – 0.5$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage ($CS, fO, SDI$)</td>
<td>2.7$V \leq V_{CC} \leq 5.5V$</td>
<td>⚫</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage ($SCK$)</td>
<td>2.7$V \leq V_{CC} \leq 5.5V$ (Notes 10, 15)</td>
<td>⚫</td>
<td>$V_{CC} – 0.5$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage ($SCK$)</td>
<td>2.7$V \leq V_{CC} \leq 5.5V$ (Notes 10, 15)</td>
<td>⚫</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Digital Input Current ($CS, fO, SDI$)</td>
<td>$0V \leq V_{IN} \leq V_{CC}$</td>
<td>⚫</td>
<td>−10</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Digital Input Current ($SCK$)</td>
<td>$0V \leq V_{IN} \leq V_{CC}$ (Notes 10, 15)</td>
<td>⚫</td>
<td>−10</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Digital Input Capacitance ($CS, fO, SDI$)</td>
<td></td>
<td>10</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Digital Input Capacitance ($SCK$)</td>
<td>(Notes 10, 17)</td>
<td>10</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage ($SDO$)</td>
<td>$I_0 = –800\mu A$ (Notes 10, 17)</td>
<td>⚫</td>
<td>$V_{CC} – 0.5$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage ($SDO$)</td>
<td>$I_0 = 1.6mA$ (Notes 10, 17)</td>
<td>⚫</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage ($SCK$)</td>
<td>$I_0 = –800\mu A$</td>
<td>⚫</td>
<td>$V_{CC} – 0.5$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage ($SCK$)</td>
<td>$I_0 = 1.6mA$</td>
<td>⚫</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>HI-Z Output Leakage ($SDO$)</td>
<td>⚫</td>
<td>−10</td>
<td>10</td>
<td>μA</td>
<td></td>
</tr>
</tbody>
</table>

**POWER REQUIREMENTS**

The ⚫ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td></td>
<td>2.7</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>Conversion Current (Note 12) Temperature Measurement (Note 12) Sleep Mode (Note 12) H-Grade</td>
<td>⚫</td>
<td>160</td>
<td>275</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>⚫</td>
<td>200</td>
<td>300</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>⚫</td>
<td>1</td>
<td>2</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>⚫</td>
<td>2.5</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>
## Digital Inputs and Digital Outputs

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ\text{C}. \) (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>( f_{EOSC} )</td>
<td>External Oscillator Frequency Range</td>
<td>(Note 16)</td>
<td>●</td>
<td>10</td>
<td>4000</td>
<td>kHz</td>
</tr>
<tr>
<td>( f_{HEO} )</td>
<td>External Oscillator High Period</td>
<td></td>
<td>●</td>
<td>0.125</td>
<td>50</td>
<td>( \mu )s</td>
</tr>
<tr>
<td>( f_{LEO} )</td>
<td>External Oscillator Low Period</td>
<td></td>
<td>●</td>
<td>0.125</td>
<td>50</td>
<td>( \mu )s</td>
</tr>
<tr>
<td>( f_{CONV,1} )</td>
<td>Conversion Time for 1x Speed Mode</td>
<td>50Hz Mode</td>
<td>●</td>
<td>157.2</td>
<td>160.3</td>
<td>163.5</td>
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<td></td>
<td></td>
<td>60Hz Mode</td>
<td></td>
<td>131</td>
<td>133.6</td>
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<td></td>
<td></td>
<td>Simultaneous 50/60Hz Mode External Oscillator</td>
<td></td>
<td>144.1</td>
<td>146.9</td>
<td>149.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(</td>
<td>41036/f_{EOSC} ) (in kHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>50Hz Mode</td>
<td></td>
<td>78.7</td>
<td>80.3</td>
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<td></td>
<td></td>
<td>60Hz Mode</td>
<td></td>
<td>65.6</td>
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<td></td>
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<td>Simultaneous 50/60Hz Mode</td>
<td></td>
<td>72.2</td>
<td>73.6</td>
<td>75.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(</td>
<td>20556/f_{EOSCK} ) (in kHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{ISCK} )</td>
<td>Internal SCK Frequency</td>
<td>Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)</td>
<td>●</td>
<td>38.4</td>
<td>( f_{EOSC}/8 )</td>
<td>kHz</td>
</tr>
<tr>
<td>( D_{ISCK} )</td>
<td>Internal SCK Duty Cycle</td>
<td>(Note 10)</td>
<td>●</td>
<td>45</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>( f_{ESCK} )</td>
<td>External SCK Frequency Range</td>
<td>(Note 10)</td>
<td>●</td>
<td>4000</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>( f_{LESCK} )</td>
<td>External SCK LOW Period</td>
<td>(Note 10)</td>
<td>●</td>
<td>125</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( f_{HESCK} )</td>
<td>External SCK High Period</td>
<td>(Note 10)</td>
<td>●</td>
<td>125</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DOUT,ISCK} )</td>
<td>Internal SCK 32-Bit Data Output Time</td>
<td>Internal Oscillator External Oscillator</td>
<td>●</td>
<td>0.81</td>
<td>0.83</td>
<td>0.85</td>
</tr>
<tr>
<td>( t_{DOUT,ESCK} )</td>
<td>External SCK 32-Bit Data Output Time</td>
<td>(Note 10)</td>
<td></td>
<td>32/( f_{ESCK} ) (in kHz)</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( t_1 )</td>
<td>( \overline{CS} )↓ to SDO Low</td>
<td></td>
<td>●</td>
<td>0</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>( t_2 )</td>
<td>( \overline{CS} )↑ to SDO Hi-Z</td>
<td></td>
<td>●</td>
<td>0</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>( t_3 )</td>
<td>( \overline{CS} )↓ to SCK↑</td>
<td>Internal SCK Mode</td>
<td></td>
<td>●</td>
<td>0</td>
<td>200</td>
</tr>
<tr>
<td>( t_4 )</td>
<td>( \overline{CS} )↓ to SCK↑</td>
<td>External SCK Mode</td>
<td></td>
<td>●</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>( t_{QMAX} )</td>
<td>SCK↓ to SDO Valid</td>
<td></td>
<td>●</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{QMIN} )</td>
<td>SDO Hold After SCK↓</td>
<td>(Note 5)</td>
<td></td>
<td>●</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>( t_5 )</td>
<td>SCK Set-Up Before ( \overline{CS} )↓</td>
<td></td>
<td>●</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_6 )</td>
<td>SCK Hold After ( \overline{CS} )↓</td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>( t_7 )</td>
<td>SDI Setup Before SCK↑</td>
<td>(Note 5)</td>
<td></td>
<td>●</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>( t_8 )</td>
<td>SDI Hold After SCK↑</td>
<td>(Note 5)</td>
<td></td>
<td>●</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** \( V_{CC} = 2.7\text{V} \) to 5.5\text{V} unless otherwise specified.

\[ V_{REFOH} = 0.6V_{REF}, \hspace{1em} V_{REF} = 0.5V_{REF} \]

\[ V_{IN} = \left| V_{IN} \right| - \left| V_{IN} \right| \]

\[ V_{IN} = \left( \left| V_{IN} \right| - \left| V_{IN} \right| \right) \]

\[ V_{IN} = \left| V_{IN} \right| - \left| V_{IN} \right| \]

where \( V_{IN} \) and \( V_{IN} \) are the selected input channels.

**Note 4:** Use internal conversion clock or external conversion clock source with \( f_{EOSC} = 307.2\text{kHz} \) unless otherwise specified.

**Note 5:** Guaranteed by design, not subject to test.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 7:** 50Hz mode (internal oscillator) or \( f_{EOSC} = 256\text{kHz} \) ±2\% (external oscillator).

**Note 8:** 60Hz mode (internal oscillator) or \( f_{EOSC} = 307.2\text{kHz} \) ±2\% (external oscillator).

**Note 9:** Simultaneous 50Hz/60Hz mode (internal oscillator) or \( f_{EOSC} = 280\text{kHz} \) ±2\% (external oscillator).

**Note 10:** The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as a digital input and the driving clock is \( f_{ESCK} \). In the internal SCK mode, the SCK pin is used as a digital output and the output clock signal during the data output is \( f_{ISCK} \).

**Note 11:** The external oscillator is connected to the \( f_{O} \) pin. The external oscillator frequency, \( f_{EOSC} \), is expressed in kHz.

**Note 12:** The converter uses its internal oscillator.

**Note 13:** The output noise includes the contribution of the internal calibration operations.

**Note 14:** Guaranteed by design and test correlation.

**Note 15:** The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is \( f_{ESCK} \) and is expressed in Hz.

**Note 16:** Refer to Applications Information section for performance vs data rate graphs.

**Note 17:** The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output.

**Note 18:** For \( V_{CC} < 3\text{V} \), \( V_{IH} \) is 2.5\text{V} for Pin \( f_{O} \).
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity
(V_{CC} = 5V, \ V_{REF} = 5V)

Integral Nonlinearity
(V_{CC} = 5V, \ V_{REF} = 2.5V)

Integral Nonlinearity
(V_{CC} = 2.7V, \ V_{REF} = 2.5V)

Total Unadjusted Error
(V_{CC} = 5V, \ V_{REF} = 5V)

Total Unadjusted Error
(V_{CC} = 5V, \ V_{REF} = 2.5V)

Total Unadjusted Error
(V_{CC} = 2.7V, \ V_{REF} = 2.5V)

Noise Histogram (6.8sps)

Noise Histogram (7.5sps)

Long-Term ADC Readings

V_{CC} = 5V, \ V_{REF} = 5V, \ V_{IN} = 0V, \ V_{IN(CM)} = 2.5V
T_{A} = 25°C, RMS Noise = 0.60\mu V
**TYPICAL PERFORMANCE CHARACTERISTICS**

**RMS Noise vs Input Differential Voltage**

- $V_{CC} = 5\text{V}$
- $V_{REF} = 5\text{V}$
- $V_{IN}(\text{CM}) = 2.5\text{V}$
- $T_A = 25^\circ\text{C}$

**RMS Noise vs $V_{IN}(\text{CM})$**

- $V_{CC} = 5\text{V}$
- $V_{REF} = 5\text{V}$
- $V_{IN} = 0\text{V}$
- $V_{IN}(\text{CM}) = \text{GND}$
- $T_A = 25^\circ\text{C}$

**RMS Noise vs Temperature ($T_A$)**

- $V_{CC} = 5\text{V}$
- $V_{REF} = 5\text{V}$
- $V_{IN} = 0\text{V}$
- $V_{IN}(\text{CM}) = \text{GND}$

**RMS Noise vs $V_{CC}$**

- $V_{REF} = 2.5\text{V}$
- $V_{IN} = 0\text{V}$
- $V_{IN}(\text{CM}) = \text{GND}$
- $T_A = 25^\circ\text{C}$

**RMS Noise vs $V_{REF}$**

- $V_{CC} = 5\text{V}$
- $V_{IN} = 0\text{V}$
- $V_{IN}(\text{CM}) = \text{GND}$
- $T_A = 25^\circ\text{C}$

**Offset Error vs $V_{IN}(\text{CM})$**

- $V_{CC} = 5\text{V}$
- $V_{REF} = 5\text{V}$
- $V_{IN} = 0\text{V}$
- $V_{IN}(\text{CM}) = \text{GND}$
- $T_A = 25^\circ\text{C}$

**Offset Error vs Temperature**

- $V_{CC} = 5\text{V}$
- $V_{REF} = 5\text{V}$
- $V_{IN} = 0\text{V}$
- $V_{IN}(\text{CM}) = \text{GND}$
- $T_A = 25^\circ\text{C}$

**Offset Error vs $V_{CC}$**

- $V_{REF} = 2.5\text{V}$
- $V_{REF} = \text{GND}$
- $V_{IN} = 0\text{V}$
- $V_{IN}(\text{CM}) = \text{GND}$
- $T_A = 25^\circ\text{C}$

**Offset Error vs $V_{REF}$**

- $V_{CC} = 5\text{V}$
- $V_{REF} = \text{GND}$
- $V_{IN} = 0\text{V}$
- $V_{IN}(\text{CM}) = \text{GND}$
- $T_A = 25^\circ\text{C}$
Typical Performance Characteristics

On-Chip Oscillator Frequency vs Temperature

On-Chip Oscillator Frequency vs VCC

PSRR vs Frequency at VCC

Sleep Mode Current vs Temperature

Conversion Current vs Output Data Rate

Integral Nonlinearity (2x Speed Mode; VCC = 5V, VREF = 5V)

Conversion Current vs Output Data Rate (READINGS/SEC)

Supply Current (µA)

Input Voltage (V)

Inl (ppm OF VREF)

TEMPERATURE (°C)

–45 –30 30 45 60 75 90

VCC = 4.1V DC ±1.4V

VREF = 2.5V

IN+ = GND

IN– = GND

fO = GND

TA = 25°C

SUPPLY CURRENT (µA)

500 450 400 350 300 250 200 150 100 50

VCC = 5V

VCC = 2.7V

fO = GND

CS = GND

SCK = NC

SDO = NC

SDI = GND

VREF = VCC

fO = EXT OSC

TA = 25°C

IN+ = GND

IN– = GND

fO = GND

TA = 25°C

FREQUENCY AT VCC (Hz)

0 20 40 60 80 100 120 140 160 180 200 220

REJECTION (dB)

–120 –100 –80 –60 –40 –20 0

TEMPERATURE (°C)

–45 –30 30 45 60 75 90

INL (ppm OF VREF)

–3 –2 –1 0 1 2

VCC = 5V

VCC = 3V

fO = GND

CS = GND

SCK = NC

SDO = NC

SDI = GND

VREF = VCC

fO = EXT OSC

TA = 25°C

IN+ = GND

IN– = GND

fO = GND

TA = 25°C

FREQUENCY AT VCC (Hz)

30600 30750 30800 30900 30100

REJECTION (dB)

–120 –100 –80 –60 –40 –20 0

FREQUENCY AT VCC (Hz)

30600 30750 30800 30900 30100

VCC = 5V

VCC = 3V

VREF = VCC

fO = EXT OSC

TA = 25°C

IN+ = GND

IN– = GND

fO = GND

TA = 25°C

Conversion Current vs Temperature

Integrated Nonlinearity (2x Speed Mode; VCC = 5V, VREF = 5V)

VCC = 5V

VCC = 2.5V

fO = GND

TA = 25°C

–45°C

INPUT VOLTAGE (V)

–2.5 –1.5 –0.5 0 0.5 1 1.5 2.5

INL (ppm OF VREF)

0

25°C, 90°C

–3 –2 –1 0 1 2
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity (2x Speed Mode; \(V_{CC} = 5\text{V}, V_{REF} = 2.5\text{V}\))

Offset Error vs \(V_{CC}\) (2x Speed Mode)

RMS Noise vs \(V_{REF}\) (2x Speed Mode)

Offset Error vs \(V_{IN(CM)}\) (2x Speed Mode)

Offset Error vs Temperature (2x Speed Mode)

PSRR vs Frequency at \(V_{CC}\) (2x Speed Mode)

Integral Nonlinearity (2x Speed Mode; \(V_{CC} = 2.7\text{V}, V_{REF} = 2.5\text{V}\))

Noise Histogram (2x Speed Mode)

RMS Noise vs \(V_{REF}\) (2x Speed Mode)

Offset Error vs \(V_{IN(CM)}\) (2x Speed Mode)

Offset Error vs Temperature (2x Speed Mode)

PSRR vs Frequency at \(V_{CC}\) (2x Speed Mode)
TYPICAL PERFORMANCE CHARACTERISTICS

PIN FUNCTIONS

GND (Pins 1, 3, 4, 5, 6, 31, 32, 33): Ground. Multiple ground pins internally connected for optimum ground current flow and VCC decoupling. Connect each one of these pins to a common ground plane through a low impedance connection. All eight pins must be connected to ground for proper operation.

NC (Pin 2): No Connection. This pin can be left floating or tied to GND.

COM (Pin 7): The Common Negative Input (IN–) for All Single-Ended Multiplexer Configurations. The voltage on CH0 to CH15 and COM pins can have any value between GND – 0.3V to VCC + 0.3V. Within these limits, the two selected inputs (IN+ and IN–) provide a bipolar input range (VIN = IN+ – IN–) from −0.5 • VREF to 0.5 • VREF. Outside this input range, the converter produces unique over-range and under-range output codes.

CH0 to CH15 (Pins 8 to 23): Analog Inputs. May be programmed for single-ended or differential mode.

MUXOUTP (Pin 24): Positive Multiplexer Output. Used to drive an external buffer/amplifier or can be shorted directly to ADCINP.

ADCINP (Pin 25): Positive ADC Input. Tie to the output of a buffer/amplifier driven by MUXOUTP or tie directly to MUXOUTP.

ADCINN (Pin 26): Negative ADC Input. Tie to the output of a buffer/amplifier driven by MUXOUTN or tie directly to MUXOUTN.

MUXOUTN (Pin 27): Negative Multiplexer Output. Used to drive an external buffer/amplifier or can be shorted directly to ADCINN.

VCC (Pin 28): Positive Supply Voltage. Bypass to GND with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor as close to the part as possible.

REF+ (Pin 29), REF– (Pin 30): Differential Reference Input. The voltage on these pins can have any value between GND and VCC as long as the reference positive input, REF+, remains more positive than the negative reference input, REF–, by at least 0.1V. The differential voltage (REF = REF+ – REF–) sets the full-scale range for all input channels. When performing an on-chip temperature measurement, the minimum value of REF = 2V.
PIN FUNCTIONS

**SDI (Pin 34):** Serial Data Input. This pin is used to select the line frequency rejection mode, 1x or 2x mode, temperature sensor, as well as the input channel. The serial data input is applied under control of the serial clock (SCK) during the data output/input operation. The first conversion following a new input or mode change is valid.

**f₀ (Pin 35):** Frequency Control Pin. Digital input that controls the internal conversion clock rate. When f₀ is connected to VCC or GND, the converter uses its internal oscillator running at 307.2kHz. The conversion clock may also be overridden by driving the f₀ pin with an external clock in order to change the output rate and the digital filter rejection null.

**CS (Pin 36):** Active LOW Chip Select. A LOW on this pin enables the digital input/output and wakes up the ADC. Following each conversion, the ADC automatically enters the Sleep mode and remains in this low power state as long as CS is HIGH. A LOW-to-HIGH transition on CS during the Data Output aborts the data transfer and starts a new conversion.

**SDO (Pin 37):** Three-State Digital Output. During the data output period, this pin is used as the serial data output. When the chip select pin is HIGH, the SDO pin is in a high impedance state. During the conversion and sleep periods, this pin is used as the conversion status output. When the conversion is in progress this pin is HIGH; once the conversion is complete SDO goes LOW. The conversion status is monitored by pulling CS LOW.

**SCK (Pin 38):** Bidirectional, Digital I/O, Clock Pin. In Internal Serial Clock Operation mode, SCK is generated internally and is seen as an output on the SCK pin. In External Serial Clock Operation mode, the digital I/O clock is externally applied to the SCK pin. The Serial Clock operation mode is determined by the logic level applied to the SCK pin at power-up and during the most recent falling edge of CS.

**Exposed Pad (Pin 39):** Ground. This pin is ground and must be soldered to the PCB ground plane. For prototyping purposes, this pin may remain floating.
Figure 1. Functional Block Diagram

TEST CIRCUITS

SDO

1.69k

CLOAD = 20pF

Hi-Z TO VOH
VOL TO VOH
VOH TO Hi-Z
**TIMING DIAGRAMS**

**Timing Diagram Using Internal SCK (SCK HIGH with CS↓)**

- CS
- SDO
- SCX
- SDI
- SLEEP
- DATA IN/OUT
- CONVERSION

---

**Timing Diagram Using External SCK (SCK LOW with CS↓)**

- CS
- SDO
- SCX
- SDI
- SLEEP
- DATA IN/OUT
- CONVERSION
Converter Operation Cycle

The LTC2498 is a multi-channel, low power, delta-sigma analog-to-digital converter with an easy to use 4-wire interface and automatic differential input current cancellation. Its operation is made up of three states (See Figure 2). The converter operating cycle begins with the conversion, followed by the sleep state and ends with the data input/output cycle. The 4-wire interface consists of serial data output (SDO), serial clock (SCK), chip select (CS) and serial data input (SDI). The interface, timing, operation cycle, and data output format is compatible with Linear’s entire family of ΔΣ converters.

Initially, at power-up, the LTC2498 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, if CS in HIGH, power consumption is reduced by two orders of magnitude. The part remains in the sleep state as long as CS is HIGH. The conversion result is held indefinitely in a static shift register while the part is in the sleep state.

Once CS is pulled LOW, the device powers up, exits the sleep mode, and enters the data input/output state. If CS is brought HIGH before the first rising edge of SCK, the device returns to the sleep state and the power is reduced. If CS is brought HIGH after the first rising edge of SCK, the data output cycle is aborted and a new conversion cycle begins. The data output corresponds to the conversion just completed. This result is shifted out on the serial data output pin (SDO) under the control of the serial clock pin (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (See Figure 3). The configuration data for the next conversion is also loaded into the device at this time. Data is loaded from the serial data input pin (SDI) on each rising edge of SCK. The data input/output cycle is concluded once 32 bits are read out of the ADC or when CS is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

Through timing control of the CS and SCK pins, the LTC2498 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming and do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Ease of Use

The LTC2498 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog inputs is straightforward. Each conversion, immediately following a newly selected input or mode, is valid and accurate to the full specifications of the device.

The LTC2498 automatically performs offset and full scale calibration every conversion cycle independent of the input channel selected. This calibration is transparent to the user and has no effect with the operation cycle described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage variation, input channel, and temperature drift.

Easy Drive Input Current Cancellation

The LTC2498 combines a high precision delta-sigma ADC with an automatic, differential, input current cancellation front end. A proprietary front end passive sampling network transparently removes the differential input current. This

Figure 2. LTC2498 State Transition Diagram
enables external RC networks and high impedance sensors to directly interface to the LTC2498 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see the Automatic Differential Input Current Cancellation section). This unique architecture does not require on-chip buffers thereby enabling signals to swing beyond ground or up to \( V_{CC} \). Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full-scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2498 automatically enters an internal reset state when the power supply voltage \( V_{CC} \) drops below approximately 2V. This feature guarantees the integrity of the conversion result, input channel selection, and serial clock mode.

When \( V_{CC} \) rises above this threshold, the converter creates an internal power-on reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel \( IN^+ = CH0, IN^- = CH1 \), simultaneous 50Hz/60Hz rejection and 1x output rate. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, or temperature selection can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for \( REF^+ \) and \( REF^- \) pins covers the entire operating range of the device (GND to \( V_{CC} \)). For correct converter operation, \( V_{REF} \) must be positive (\( REF^+ > REF^- \)).

The LTC2498 differential reference input range is 0.1V to \( V_{CC} \). For the simplest operation, \( REF^+ \) can be shorted to \( V_{CC} \) and \( REF^- \) can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter’s effective resolution. On the other hand, a decreased reference will improve the converter’s overall INL performance.

Input Voltage Range

The analog input is truly differential with an absolute, common mode range for CH0 to CH15 and COM input pins extending from GND – 0.3V to \( V_{CC} + 0.3V \). Outside these limits, the ESD projection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2498 converts the bipolar differential input signal \( V_{IN} = IN^+ + IN^- \) (where \( IN^+ \) and \( IN^- \) are the selected input channels), from \( -FS = -0.5 \times V_{REF} \) to \( +FS = 0.5 \times V_{REF} \) where \( V_{REF} = REF^- - REF^+ \). Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes.

Signals applied to the input (CH0 to CH15, COM) may extend 300mV below ground and above \( V_{CC} \). In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if \( V_{REF} = 5V \). This error has a very strong temperature dependency.

MUXOUT/ADCIN

The output of the multiplexer (MUXOUT) and the input to the ADC (ADCIN) can be used to perform input signal conditioning on any of the selected input channels or simply shorted together for direct digitization. If an external amplifier is used, the LTC2498 automatically calibrates both the offset and drift of this circuit and the Easy Drive sampling scheme enables a wide variety of amplifiers to be used.

In order to achieve optimum performance, if an external amplifier is not used, short these pins directly together (ADCINP to MUXOUTP and ADCINN to MUXOUTN) and minimize their capacitance to ground.
Applications Information

Serial Interface Pins

The LTC2498 transmits the conversion result, reads the input configuration, and receives a start of conversion command through a synchronous 3- or 4-wire interface. During the conversion and sleep states, this interface can be used to access the converter status. During the data output state, it is used to read the conversion result, program the input channel, rejection frequency, speed multiplier, and select the temperature sensor.

Serial Clock Input/Output (SCK)

The serial clock pin (SCK) is used to synchronize the data input/output transfer. Each bit is shifted out of the SDO pin on the falling edge of SCK and data is shifted into the SDI pin on the rising edge of SCK.

The serial clock pin (SCK) can be configured as either a master (SCK is an output generated internally) or a slave (SCK is an input and applied externally). Master mode (internal SCK) is selected by simply floating the SCK pin. Slave mode (external SCK) is selected by driving SCK LOW during power-up and each falling edge of CS. Specific details of these SCK modes are described in the Serial Interface Timing Modes section.

Serial Data Output (SDO)

The serial data output pin (SDO) provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When CS is HIGH, the SDO driver is switched to a high impedance state in order to share the data output line with other devices. If CS is brought LOW during the conversion phase, the EOC bit (SDO pin) will be driven HIGH. Once the conversion is complete, if CS is brought LOW, EOC will be driven LOW indicating the conversion is complete and the result is ready to be shifted out of the device.

Chip Select (CS)

The active low CS pin is used to test the conversion status, enable I/O data transfer, initiate a new conversion, control the duration of the sleep state, and set the SCK mode.

At the conclusion of a conversion cycle, while CS is HIGH, the device remains in a low power sleep state where the supply current is reduced several orders of magnitude. In order to exit the sleep state and enter the data output state, CS must be pulled LOW. Data is now shifted out the SDO pin under control of the SCK pin as described previously.

A new conversion cycle is initiated either at the conclusion of the data output cycle (all 32 data bits read) or by pulling CS HIGH any time between the first and 32nd rising edges of the serial clock (SCK). In this case, the data output is aborted and a new conversion begins.

Serial Data Input (SDI)

The serial data input (SDI) is used to select the input channel, rejection frequency, speed multiplier and to access the integrated temperature sensor. Data is shifted into the device during the data output/input state on the rising edge of SCK while CS is LOW.

Output Data Format

The LTC2498 serial output stream is 32 bits long. The first bit indicates the conversion status, the second bit is always zero, and the third bit conveys sign information. The next 24 bits are the conversion result, MSB first. The remaining 5 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.

Bit 31 (first output bit) is the end of conversion (EOC) indicator. This bit is available on the SDO pin during the conversion and sleep states whenever CS is LOW. This bit is HIGH during the conversion cycle, goes LOW once the conversion is complete, and is Hi-Z when CS is HIGH.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If the selected input (V_{IN} = V_{IN+} – V_{IN-}) is greater than 0V, this bit is HIGH. If V_{IN} < 0, this bit is LOW.

Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 29 also provides underrange and overrange indication. If both Bit 29 and Bit 28 are HIGH, the differential input voltage is above...
APPLICATIONS INFORMATION

+FS. If both Bit 29 and Bit 28 are LOW, the differential input voltage is below –FS. The function of these bits is summarized in Table 1.

Table 1. LTC2498 Status Bits

<table>
<thead>
<tr>
<th>Input Range</th>
<th>Bit 31 EOC</th>
<th>Bit 30 DMY</th>
<th>Bit 29 SIG</th>
<th>Bit 28 MSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN} \geq 0.5 \cdot V_{REF}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>$0V \leq V_{IN} &lt; 0.5 \cdot V_{REF}$</td>
<td>0</td>
<td>0</td>
<td>1/0</td>
<td>0</td>
</tr>
<tr>
<td>$-0.5 \cdot V_{REF} \leq V_{IN} &lt; 0V$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$V_{IN} &lt; -0.5 \cdot V_{REF}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bits 28 to 5 are the 24-bit conversion result MSB first. Bit 5 is the least significant bit (LSB24).

Bits 4 to 0 are sub LSBs below the 24-bit level. Bits 4 to 0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever CS is HIGH, SDO remains high impedance and SCK is ignored.

In order to shift the conversion result out of the device, CS must first be driven LOW. EOC is seen at the SDO pin of the device once CS is pulled LOW. EOC changes in real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 (EOC) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the rising edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as EOC (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the IN+ and IN– pins remains between –0.3V and $V_{CC} + 0.3V$ (absolute maximum operating range) a conversion result is generated for any differential input voltage $V_{IN}$ from $-FS = -0.5 \cdot V_{REF}$ to $+FS = 0.5 \cdot V_{REF}$. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to $+FS + 1$LSB. For differential input voltages below –FS, the conversion result is clamped to the value $–FS – 1$LSB.

Figure 3. Channel Selection, Configuration Selection and Data Output Timing
The LTC2498 serial input word is 13 bits long and contains two distinct sets of data. The first set (SGL, ODD, A2, A1, A0) is used to select the input channel. The second set of data (IM, FA, FB, SPD) is used to select the frequency rejection, speed mode (1x, 2x), and temperature measurement.

After power-up, the device initiates an internal reset cycle which sets the input channel to CH0–CH1 (IN+ = CH0, IN– = CH1), the frequency rejection to simultaneous 50Hz/60Hz, and 1x output rate (auto-calibration enabled). The first conversion automatically begins at power-up using this default configuration. Once the conversion is complete, a new word may be written into the device.

The first 3 bits shifted into the device consist of two preenable bits and one enable bit. As demonstrated in Figure 3, the first three bits shifted into the device enable the device configuration and input channel selection. Valid settings for these three bits are 000, 100 and 101. Other combinations should be avoided. If the first three bits are 000 or 100, the following data is ignored (don’t care) and the previously selected input channel and configuration remain valid for the next conversion.

If the first 3 bits shifted into the device are 101, then the next 5 bits select the input channel for the next conversion cycle, see Table 3.

The first input bit following the 101 sequence (SGL) determines if the input selection is differential (SGL = 0) or single-ended (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input. For SGL = 1, one of 16 channels is selected as the positive input. The negative input is COM for all single ended operations. The remaining 4 bits (ODD, A2, A1, A0) determine which channel(s) is/are selected and the polarity (for a differential input).

The next serial input bit immediately following the input channel selection is the enable bit for the conversion configuration (EN2). If this bit is set to 0, then the next conversion is performed using the previously selected converter configuration. This is useful in systems using the same rejection/speed for all input channels and for backward compatibility with the LTC2418/LTC2414 families of delta sigma ADCs.

A new configuration can be loaded into the device by setting EN2 = 1, see Table 4. The first bit (IM) is used to select the internal temperature sensor. If IM = 1, the following conversion will be performed on the internal temperature sensor rather than the selected input channel. The next 2 bits (FA and FB) are used to set the rejection frequency. The final bit (SPD) is used to select either the 1x output rate if SPD = 0 (auto-calibration is enabled and the offset is continuously calibrated and removed from

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**Table 2. Output Data Format**

<table>
<thead>
<tr>
<th>Differential Input Voltage $V_{IN}^*$</th>
<th>Bit 31 EOC</th>
<th>Bit 30 DMY</th>
<th>Bit 29 SIG</th>
<th>Bit 28 MSB</th>
<th>Bit 27</th>
<th>Bit 26</th>
<th>Bit 25</th>
<th>...</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}^* \geq 0.5 \cdot V_{REF}^{**}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>...</td>
<td>0</td>
</tr>
<tr>
<td>$0.5 \cdot V_{REF}^{**} – 1LSB$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>...</td>
<td>1</td>
</tr>
<tr>
<td>$0.25 \cdot V_{REF}^{**}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>...</td>
<td>0</td>
</tr>
<tr>
<td>$0.25 \cdot V_{REF}^{**} – 1LSB$</td>
<td>0</td>
<td>0</td>
<td>1/0***</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<td>$-1LSB$</td>
<td>0</td>
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<td>1</td>
<td>...</td>
<td>1</td>
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<td>$-0.25 \cdot V_{REF}^{**}$</td>
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<td>$-0.25 \cdot V_{REF}^{**} – 1LSB$</td>
<td>0</td>
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<td>1</td>
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<tr>
<td>$-0.5 \cdot V_{REF}^{**}$</td>
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<td>0</td>
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<td>0</td>
<td>...</td>
<td>0</td>
</tr>
<tr>
<td>$V_{IN}^* &lt; -0.5 \cdot V_{REF}^{**}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>...</td>
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</table>

*The differential input voltage $V_{IN} = IN+ – IN–$, **The differential reference voltage $V_{REF} = REF+ – REF–$. ***The sign bit changes state during the 0 output code when the device is operating in the 2x speed mode.
## Table 3. Channel Selection

<table>
<thead>
<tr>
<th>SGL</th>
<th>ODD/ SIGN</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>COM</th>
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<tr>
<td>*0</td>
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<td>0</td>
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*Default at power-up*
the final conversion result) or the 2x output rate if SPD = 1 (offset calibration disabled, multiplexing output rates up to 15Hz with no latency). When IM = 1 (temperature measurement), SPD will be ignored and the device will operate in 1x mode. The configuration remains valid until a new input word with EN = 1 (the first 3 bits are 101) and EN2 = 1 is shifted into the device.

**Rejection Mode (FA, FB)**

The LTC2498 includes a high accuracy on-chip oscillator with no required external components. Coupled with an integrated 4th order digital lowpass filter, the LTC2498 rejects line frequency noise. In the default mode, the LTC2498 simultaneously rejects 50Hz and 60Hz by at least 87dB. If more rejection is required, the LTC2498 can be configured to reject 50Hz or 60Hz to better than 110dB.

**Speed Mode (SPD)**

Every conversion cycle, two conversions are combined to remove the offset (default mode). This result is free from offset and drift. In applications where the offset is not critical, the auto-calibration feature can be disabled with the benefit of twice the output rate. While operating in the 2x mode (SPD = 1), the linearity and full-scale errors are unchanged from the 1x mode performance. In both the 1x and 2x mode there is no latency. This enables input steps or multiplexer changes to settle in a single conversion cycle easing system overhead and increasing the effective conversion rate. During temperature measurements, the 1x mode is always used independent of the value of SPD.

**Temperature Sensor**

The LTC2498 includes an integrated temperature sensor. The temperature sensor is selected by setting IM = 1. During temperature readings, MUXOUTN/MUXOUTP remains connected to the selected input channel. The ADC internally connects to the temperature sensor and performs a conversion.

The digital output is proportional to the absolute temperature of the device. This feature allows the converter to perform cold junction compensation for external thermocouples or continuously remove the temperature effects of external sensors.

The internal temperature sensor output is 28mV at 27°C (300°K), with a slope of 93.5µV/°C independent of VREF.
APPLICATIONS INFORMATION

Slope calibration is not required if the reference voltage \( V_{\text{REF}} \) is known. A 5V reference has a slope of 314 LSBs/\(^\circ\)C. The temperature is calculated from the output code \( \text{DATAOUT}_{24} \) for a 5V reference using the following formula:

\[
T_K = \frac{\text{DATAOUT}_{24}}{314}\text{ in Kelvin}
\]

If a different value of \( V_{\text{REF}} \) is used, the temperature output is:

\[
T_K = \frac{\text{DATAOUT}_{24} \cdot V_{\text{REF}}}{1570}\text{ in Kelvin}
\]

If the value of \( V_{\text{REF}} \) is not known, the slope is determined by measuring the temperature sensor at a known temperature \( T_N \) (in °K) and using the following formula:

\[
\text{SLOPE} = \frac{\text{DATAOUT}_{24}}{T_N}
\]

This value of slope can be used to calculate further temperature readings using:

\[
T_K = \frac{\text{DATAOUT}_{24}}{\text{SLOPE}}
\]

All Kelvin temperature readings can be converted to \( T_C \) (°C) using the fundamental equation:

\[
T_C = T_K - 273
\]

SERIAL INTERFACE TIMING MODES

The LTC2498’s 4-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 3- or 4-wire I/O, single cycle or continuous conversion. The following sections describe each of these timing modes in detail. In all cases, the converter can use the internal oscillator \( (f_O = \text{LOW or } f_O = \text{HIGH}) \) or an external oscillator connected to the \( f_O \) pin. For each mode, the operating cycle, data input format, data output format, and performance remain the same. Refer to Table 5 for a summary.

Table 5. LTC2498 Interface Timing Modes

<table>
<thead>
<tr>
<th>CONFIGURATION</th>
<th>SCK SOURCe</th>
<th>CONVERSION CYCLE CONTROL</th>
<th>DATA OUTPUT CONTROL</th>
<th>CONNECTION AND WAVEFORMS</th>
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</thead>
<tbody>
<tr>
<td>External SCK, Single Cycle Conversion</td>
<td>External</td>
<td>CS and SCK</td>
<td>CS and SCK</td>
<td>Figures 6, 7</td>
</tr>
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<td>External SCK, 3-Wire I/O</td>
<td>External</td>
<td>SCK</td>
<td>SCK</td>
<td>Figure 8</td>
</tr>
<tr>
<td>Internal SCK, Single Cycle Conversion</td>
<td>Internal</td>
<td>CS↓</td>
<td>CS↓</td>
<td>Figures 9, 10</td>
</tr>
<tr>
<td>Internal SCK, 3-Wire I/O, Continuous Conversion</td>
<td>Internal</td>
<td>Continuous</td>
<td>Internal</td>
<td>Figure 11</td>
</tr>
</tbody>
</table>

Figure 4. Internal PTAT Digital Output vs Temperature

Figure 5. Absolute Temperature Error
**APPLICATIONS INFORMATION**

**External Serial Clock, Single Cycle Operation**

This timing mode uses an external serial clock to shift out the conversion result and CS to monitor and control the state of the conversion cycle, see Figure 6.

The external serial clock mode is selected during the power-up sequence and on each falling edge of CS. In order to enter and remain in the external SCK mode of operation, SCK must be driven LOW both at power-up and on each CS falling edge. If SCK is HIGH on the falling edge of CS, the device will switch to the internal SCK mode.

The serial data output pin (SDO) is Hi-Z as long as CS is HIGH. At any time during the conversion cycle, CS may be pulled LOW in order to monitor the state of the converter. While CS is LOW, EOC is output to the SDO pin.

EOC = 1 while a conversion is in progress and EOC = 0 if the conversion is complete and the device is in the sleep state. Independent of CS, the device automatically enters the sleep state once the conversion is complete; however, in order to reduce the power, CS must be HIGH.

When the device is in the sleep state, its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while CS is LOW. The input data is then shifted in via the SDI pin on each rising edge of SCK (including the first rising edge). The channel selection and converter configuration mode will be used for the following conversion cycle. If the input channel or converter configuration is changed during this I/O cycle, the new settings take effect on the conversion cycle following the data input/output cycle. The output data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. EOC can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion and SDO goes HIGH (EOC = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, CS may remain LOW and EOC monitored as an end-of-conversion interrupt.

![Figure 6. External Serial Clock, Single Cycle Operation](image)
APPLICATIONS INFORMATION

Typically, \( CS \) remains LOW during the data output/input state. However, the data output state may be aborted by pulling \( CS \) HIGH any time between the 1st falling edge and the 32nd falling edge of SCK, see Figure 7. On the rising edge of \( CS \), the device aborts the data output state and immediately initiates a new conversion. In order to program a new input channel, 8 SCK clock pulses are required. If the data output sequence is aborted prior to the 8th falling edge of SCK, the new input data is ignored and the previously selected input channel remains valid. If the rising edge of \( CS \) occurs after the 8th falling edge of SCK, the new input channel is loaded and valid for the next conversion cycle. If \( CS \) goes HIGH between the 8th falling edge and the 16th falling edge of SCK, the new channel is still loaded, but the converter configuration remains unchanged. In order to program both the input channel and converter configuration, \( CS \) must go HIGH after the 16th falling edge of SCK (at this point all data has been shifted into the device).

External Serial Clock, 3-Wire I/O

This timing mode uses a 3-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 8. \( CS \) is permanently tied to ground, simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is typically concluded 4ms after \( V_{CC} \) exceeds 2V. The level applied to SCK at this time determines if SCK is internally generated or externally applied. In order to enter the external SCK mode, SCK must be driven LOW prior to the end of the POR cycle.

Since \( CS \) is tied LOW, the end-of-conversion (EOC) can be continuously monitored at the SDO pin during the convert and sleep states. EOC may be used as an interrupt to an external controller. EOC = 1 while the conversion is in

![Figure 7. External Serial Clock, Reduced Output Data Length and Valid Channel Selection](image-url)
progress and $\text{EOC} = 0$ once the conversion is complete. On the falling edge of $\text{EOC}$, the conversion result is loading into an internal static shift register. The output data can now be shifted out the SDO pin under control of the externally applied SCK signal. Data is updated on the falling edge of SCK. The input data is shifted into the device through the SDI pin on the rising edge of SCK. On the 32nd falling edge of SCK, SDO goes HIGH, indicating a new conversion has begun. This data now serves as $\text{EOC}$ for the next conversion.

**Internal Serial Clock, Single Cycle Operation**

This timing mode uses the internal serial clock to shift out the conversion result and CS to monitor and control the state of the conversion cycle, see Figure 9.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating or pulled HIGH before the conclusion of the POR cycle and prior to each falling edge of \( \overline{CS} \). An internal weak pull-up resistor is active on the SCK pin during the falling edge of \( \overline{CS} \); therefore, the internal SCK mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as \( \overline{CS} \) is HIGH. At any time during the conversion cycle, \( \overline{CS} \) may be pulled LOW in order to monitor the state of the converter. Once \( \overline{CS} \) is pulled LOW, SCK goes LOW and EOC is output to the SDO pin. EOC = 1 while the conversion is in progress and EOC = 0 if the device is in the sleep state.

When testing EOC, if the conversion is complete (EOC = 0), the device will exit sleep state. In order to return to the sleep state and reduce the power consumption, \( \overline{CS} \) must be pulled HIGH before the device pulls SCK HIGH. When the device is using its own internal oscillator (\( f_0 \) is tied LOW), the first rising edge of SCK occurs 12\( \mu \)s (\( t_{EOCTEST} = 12\mu s \)) after the falling edge of \( \overline{CS} \). If \( f_0 \) is driven by an external oscillator of frequency \( f_{EOSC} \), then \( t_{EOCTEST} = 3.6/f_{EOSC} \).

If \( \overline{CS} \) remains LOW longer than \( t_{EOCTEST} \), the first rising edge of SCK will occur and the conversion result is shifted out the SDO pin on the falling edge of SCK. The serial input word (SDI) is shifted into the device on the rising edge of SCK.

After the 32nd rising edge of SCK a new conversion automatically begins. SDO goes HIGH (EOC = 1) and SCK
remains HIGH for the duration of the conversion cycle. Once the conversion is complete, the cycle repeats.

Typically, CS remains LOW during the data output state. However, the data output state may be aborted by pulling CS HIGH any time between the 1st rising edge and the 32nd falling edge of SCK, see Figure 10. On the rising edge of CS, the device aborts the data output state and immediately initiates a new conversion. In order to program a new input channel, 8 SCK clock pulses are required. If the data output sequence is aborted prior to the 8th falling edge of SCK, the new input data is ignored and the previously selected input channel remains valid. If the rising edge of CS occurs after the 8th falling edge of SCK, the new input channel is loaded and valid for the next conversion cycle. If CS goes HIGH between the 8th falling edge and the 16th falling edge of SCK, the new channel is still loaded, but the converter configuration remains unchanged. In order to program both the input channel and converter configuration, CS must go HIGH after the 16th falling edge of SCK (at this point all data has been shifted into the device).

**Internal Serial Clock, 3-Wire I/O, Continuous Conversion**

This timing mode uses a 3-wire interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 11. In this case, CS is permanently tied to ground, simplifying the user interface or transmission over an isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 4ms after VCC exceeds 2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is floating or driven HIGH.

During the conversion, the SCK and the serial data output pin (SDO) are HIGH (EOC = 1). Once the conversion is complete, SCK and SDO go LOW (EOC = 0) indicating the conversion has finished and the device has entered the sleep state. The device remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting and inputting data.
Figure 10. Internal Serial Clock, Reduced Data Output Length with Valid Channel and Configuration Selection

Figure 11. Internal Serial Clock, Continuous Operation
APPLICATIONS INFORMATION

The input data is shifted through the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out the SDO pin on the falling edge of SCK. The data input/output cycle is concluded and a new conversion automatically begins after the 32nd rising edge of SCK. During the next conversion, SCK and SDO remain HIGH until the conversion is complete.

The Use of a 10k Pull-Up on SCK for Internal SCK Selection

If CS is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state if SCK is floating. This will cause the device to exit the internal SCK mode on the next falling edge of CS. This can be avoided by adding an external 10k pull-up resistor to the SCK pin.

Whenever SCK is LOW, the LTC2498’s internal pull-up at SCK is disabled. Normally, SCK is not externally driven if the device is operating in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If the driver goes Hi-Z after outputting a LOW signal, the internal pull-up is disabled. An external 10k pull-up resistor prevents the device from exiting the internal SCK mode under this condition.

A similar situation may occur during the sleep state when CS is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state (EOC = 0), SCK will go LOW. If CS goes HIGH before the time to EOCTEST, the internal pull-up is activated. If SCK is heavily loaded, the internal pull-up may not restore SCK to a HIGH state before the next falling edge of CS. The external 10k pull-up resistor prevents the device from exiting the internal SCK mode under this condition.

Digital Signal Levels

The LTC2498’s digital interface is easy to use. Its digital inputs (SDI, fO, CS, and SCK in external serial clock mode) accept standard CMOS logic levels. Internal hysteresis circuits can tolerate edge transition times as slow as 100µs.

The digital input signal range is 0.5V to VCC – 0.5V. During transitions, the CMOS input circuits draw dynamic current. For optimal performance, application of signals to the serial data interface should be reserved for the sleep and data output periods.

During the conversion period, overshoot and undershoot of fast digital signals applied to both the serial digital interface and the external oscillator pin (fO) may degrade the converter performance. Undershoot and overshoot occur due to impedance mismatch of the circuit board trace at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to the input pin. For reference, on a regular FR-4 board, the propagation delay is approximately 183ps/inch. In order to prevent overshoot, a driver with a 1ns transition time must be connected to the converter through a trace shorter than 2.5 inches. This becomes difficult when shared control lines are used and multiple reflections occur.

Parallel termination near the input pin of the LTC2498 will eliminate this problem, but will increase the driver power dissipation. A series resistor from 27Ω to 54Ω (depending on the trace impedance and connection) placed near the driver will also eliminate over/undershoot without additional driver power dissipation.

For many applications, the serial interface pins (SCK, SDI, CS, fO) remain static during the conversion cycle and no degradation occurs. On the other hand, if an external oscillator is used (fO driven externally) it is active during the conversion cycle. Moreover, the digital filter rejection is minimal at the clock rate applied to fO. Care must be taken to ensure external inputs and reference lines do not cross this signal or run near it. These issues are avoided when using the internal oscillator.

PRESEVING THE CONVERTER ACCURACY

The LTC2498 is designed to reduce as much as possible sensitivity to device decoupling, PCB layout, anti-aliasing circuits, line frequency perturbations, and temperature sensitivity. In order to achieve maximum performance a few simple precautions should be observed.
Driving the Input and Reference

The input and reference pins of the LTC2498 are connected directly to a switched capacitor network. Depending on the relationship between the differential input voltage and the differential reference voltage, these capacitors are switched between these four pins. Each time a capacitor is switched between two of these pins, a small amount of charge is transferred. A simplified equivalent circuit is shown in Figure 12.

When using the LTC2498’s internal oscillator, the input capacitor array is switched at 123kHz. The effect of the charge transfer depends on the circuitry driving the input/reference pins. If the total external RC time constant is less than 580ns the errors introduced by the sampling process are negligible since complete settling occurs.

Typically, the reference inputs are driven from a low impedance source. In this case complete settling occurs even with large external bypass capacitors. The inputs (CHO to CH15, COM), on the other hand, are typically driven from larger source resistances. Source resistances up to 10k may interface directly to the LTC2498 and settle completely; however, the addition of external capacitors at the input terminals in order to filter unwanted noise (anti-aliasing) results in incomplete settling.

The LTC2498 offers two methods of removing these errors. The first is an automatic differential input current cancellation (Easy Drive) and the second is the insertion of buffer between the MUXOUT and ADCIN pins, thus isolating the input switching from the source resistance.

Automatic Differential Input Current Cancellation

In applications where the sensor output impedance is low (up to 10kΩ with no external bypass capacitor or up to 500Ω with 0.001µF bypass), complete settling of the input occurs. In this case, no errors are introduced and direct digitization is possible.

For many applications, the sensor output impedance combined with external input bypass capacitors produces RC time constants much greater than the 580ns required for 1ppm accuracy. For example, a 10k bridge driving a 0.1µF capacitor has a time constant an order of magnitude greater than the required maximum.

The LTC2498 uses a proprietary switching algorithm that forces the average differential input current to zero.

![Figure 12. LTC2498 Equivalent Analog Input Circuit](image-url)
independent of external settling errors. This allows direct
digitization of high impedance sensors without the need
of buffers.

The switching algorithm forces the average input current
on the positive input (I_{IN^+}) to be equal to the average input
current in the negative input (I_{IN^-}). Over the complete
conversion cycle, the average input current (I_{IN^+} – I_{IN^-})
is zero. While the differential input current is zero, the
common mode input current (I_{IN^+} + I_{IN^-})/2 is proportional
to the difference between the common mode input voltage
(V_{IN(CM)}) and the common mode reference voltage
(V_{REF(CM)}).

In applications where the input common mode voltage is
equal to the reference common mode voltage, as in the
case of a balanced bridge, both the differential and com-
mon mode input current are zero. The accuracy of the
converter is not compromised by settling errors.

In applications where the input common mode voltage is
constant but different from the reference common mode
voltage, the differential input current remains zero while
the common mode input current is proportional to the
difference between V_{IN(CM)} and V_{REF(CM)}. For a reference
commom mode voltage of 2.5V and an input common mode
of 1.5V, the common mode input current is approximately
0.74µA (in simultaneous 50Hz/60Hz rejection mode). This
common mode input current does not degrade the accuracy
if the source impedances tied to IN^+ and IN^- are matched.
Mismatches in source impedance lead to a fixed offset
error but do not affect the linearity or full scale reading.
A 1% mismatch in a 1k source resistance leads to a 74µV
shift in offset voltage.

In applications where the common mode input voltage
varies as a function of the input signal level (single ended
type sensors), the common mode input current varies
proportionally with input voltage. For the case of balanced
input impedances, the common mode input current effects
are rejected by the large CMRR of the LTC2498, leading
to little degradation in accuracy. Mismatches in source
impedances lead to gain errors proportional to the dif-
ference between the common mode input and common
mode reference. 1% mismatches in 1k source resistances
lead to gain errors on the order of 15ppm. Based on the

stability of the internal sampling capacitors and the ac-
curacy of the internal oscillator, a one-time calibration will
remove this error.

In addition to the input sampling current, the input ESD
protection diodes have a temperature dependent leakage
current. This current, nominally 1nA (±10nA max) results
in a small offset shift. A 1k source resistance will create a
1µV typical and a 10µV maximum offset voltage.

**Automatic Offset Calibration of External Buffers/
Amplifiers**

In addition to the Easy Drive input current cancellation,
the LTC2498 enables an external amplifier to be inserted
between the multiplexer output and the ADC input, see
Figure 13. This is useful in applications where balanced
source impedances are not possible. One pair of external
buffers/amplifiers can be shared between all 17 analog
inputs. The LTC2498 performs an internal offset calibration
every conversion cycle in order to remove the offset and
drift of the ADC. This calibration is performed through a
combination of front end switching and digital process-
ing. Since the external amplifier is placed between the
multiplexer and the ADC, it is inside this correction loop.
This results in automatic offset correction and offset drift
removal of the external amplifier.

![Figure 13. External Buffers Provide High Impedance Inputs and
Amplifier Offsets are Automatically Cancelled.](image-url)
APPLICATIONS INFORMATION

The LTC6078 is an excellent amplifier for this function. It operates with supply voltages as low as 2.7V and its noise level is 18nV/√Hz. The Easy Drive input technology of the LTC2498 enables an RC network to be added directly to the output of the LTC6078. The capacitor reduces the magnitude of the current spikes seen at the input to the ADC and the resistor isolates the capacitor load from the op-amp output enabling stable operation.

Reference Current

Similar to the analog inputs, the LTC2498 samples the differential reference pins (REF+ and REF-) transferring small amounts of charge to and from these pins, thus producing a dynamic reference current. If incomplete settling occurs (as a function the reference source resistance and reference bypass capacitance) linearity and gain errors are introduced.

For relatively small values of external reference capacitance (CREF < 1nF), the voltage on the sampling capacitor settles for reference impedances of many kΩ (if CREF = 100pF up to 10k will not degrade the performance), see Figures 14, 15.

In cases where large bypass capacitors are required on the reference inputs (CREF > 0.01µF) full-scale and linearity errors are proportional to the value of the reference resistance. Every ohm of reference resistance produces a full-scale error of approximately 0.5ppm (while operating in simultaneous 50Hz/60Hz mode), see Figures 16 and 17. If the input common mode voltage is equal to the reference common mode voltage, a linearity error of approximately 0.67ppm per 100Ω of reference resistance results, see Figure 18. In applications where the input and reference common mode voltages are different, the errors increase. A 1V difference in between common mode input and common mode reference results in a 6.7ppm INL error for every 100Ω of reference resistance.

In addition to the reference sampling charge, the reference ESD projection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max) results in a small gain error. A 100Ω reference resistance will create a 0.5µV full scale error.

Normal Mode Rejection and Anti-Aliasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversample ratio, the LTC2498 significantly simplifies anti-aliasing filter requirements. Additionally, the input current cancellation feature allows external lowpass filtering without degrading the DC performance of the device.
The SINC⁴ digital filter provides excellent normal mode rejection at all frequencies except DC and integer multiples of the modulator sampling frequency (fₛ), see Figures 19 and 20. The modulator sampling frequency is fₛ = 15,360Hz while operating with its internal oscillator and fₛ = FEOSC/20 when operating with an external oscillator of frequency FEOSC.

When using the internal oscillator, the LTC2498 is designed to reject line frequencies. As shown in Figure 21, rejection nulls occur at multiples of frequency f_N, where f_N is determined by the input control bits FA and FB (f_N = 50Hz or 60Hz or 55Hz for simultaneous rejection). Multiples of the modulator sampling rate (fₛ = f_N • 256) only reject
noise to 15dB (see Figure 22), if noise sources are present at these frequencies anti-aliasing will reduce their effects.

The user can expect to achieve this level of performance using the internal oscillator, as shown in Figures 23, 24, and 25. Measured values of normal mode rejection are shown superimposed over the theoretical values in all three rejection modes.

Traditional high order delta-sigma modulators suffer from potential instabilities at large input signal levels. The proprietary architecture used for the LTC2498 third order modulator resolves this problem and guarantees stability with input signals 150% of full-scale. In many industrial applications, it is not uncommon to have microvolt level signals superimposed over unwanted volt level error sources with several volts of peak-to-peak
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noise. Figures 26 and 27 show measurement results for the rejection of a 7.5V peak-to-peak noise source (150% of full scale) applied to the LTC2498. From these curves, it is shown that the rejection performance is maintained even in extremely noisy environments.

Using the 2x speed mode of the LTC2498 alters the rejection characteristics around DC and multiples of f_S. The device bypasses the offset calibration in order to increase the output rate. The resulting rejection plots are shown in Figures 28 and 29. 1x type frequency rejection can be achieved using the 2x mode by performing a running average of the conversion results, see Figure 30.

Output Data Rate

When using its internal oscillator, the LTC2498 produces up to 7.5 samples per second (sps) with a notch frequency of 60Hz. The actual output data rate depends upon the length of the sleep and data output cycles which are controlled by the user and can be made insignificantly short. When operating with an external conversion clock (f_O connected to an external oscillator), the LTC2498 output data rate can be increased. The duration of the conversion cycle is 41036/f_EOSC. If f_EOSC = 307.2kHz, the converter behaves as if the internal oscillator is used.

An increase in f_EOSC over the nominal 307.2kHz will translate into a proportional increase in the maximum output data rate (up to a maximum of 100sps). The increase in output rate leads to degradation in offset, full-scale error, and effective resolution as well as a shift in frequency rejection. When using the integrated temperature sensor, the internal oscillator should be used (f_O = 0) or an external oscillator applied to f_O, f_EOSC, should be set to 307.2kHz Max.

A change in f_EOSC results in a proportional change in the internal notch position. This leads to reduced differential
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mode rejection of line frequencies. The common mode rejection of line frequencies remains unchanged, thus fully differential input signals with a high degree of symmetry on both the IN+ and IN– pins will continue to reject line frequency noise.

An increase in fEOSC also increases the effective dynamic input and reference current. External RC networks will continue to have zero differential input current, but the time required for complete settling (580ns for fEOSC = 307.2kHz) is reduced, proportionally.

Once the external oscillator frequency is increased above 1MHz (a more than 3x increase in output rate) the effectiveness of internal auto calibration circuits begins to degrade. This results in larger offset errors, full scale errors, and decreased resolution, see Figures 31 to 38.

Figure 30. Input Normal Mode Rejection 2x Speed Mode with and Without Running Averaging

Figure 31. Offset Error vs Output Data Rate and Temperature

Figure 32. +FS Error vs Output Data Rate and Temperature

Figure 33. –FS Error vs Output Data Rate and Temperature

Figure 34. Resolution (NoiseRMS ≤ 1LSB) vs Output Data Rate and Temperature

Figure 35. Resolution (INLMAX ≤ 1LSB) vs Output Data Rate and Temperature
Applications Information

Figure 36. Offset Error vs Output Data Rate and Reference Voltage

Figure 37. Resolution (NoiseRMS ≤ 1LSB) vs Output Data Rate and Reference Voltage

Figure 38. Resolution (INLMAX ≤ 1LSB) vs Output Data Rate and Reference Voltage
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHAD ED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
7. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
8. DRAWING NOT TO SCALE
9. ALL DIMENSIONS ARE IN MILLIMETERS
10. SHAD ED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)

RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED
## REVISION HISTORY

(Revision history begins at Rev D)

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<td>Update Tables 1 and 2</td>
<td>17, 18</td>
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<tr>
<td>E</td>
<td>07/10</td>
<td>Revised Typical Application drawing</td>
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<td></td>
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<td>Added Note 18 to Digital Inputs and Digital Outputs section</td>
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<td>F</td>
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<td>Added H-Grade</td>
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Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
TYPICAL APPLICATION

External Buffers Provide High Impedance Inputs and Amplifier Offsets Are Automatically Cancelled

![Circuit Diagram]

**RELATED PARTS**

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<th>DESCRIPTION</th>
<th>COMMENTS</th>
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<tbody>
<tr>
<td>LT1236A-5</td>
<td>Precision Bandgap Reference, 5V</td>
<td>0.05% Max Initial Accuracy, 5ppm/°C Drift</td>
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<tr>
<td>LT1460</td>
<td>Micropower Series Reference</td>
<td>0.075% Max Initial Accuracy, 10ppm/°C Max Drift</td>
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<tr>
<td>LT1790</td>
<td>Micropower SOT-23 Low Dropout Reference Family</td>
<td>0.05% Max Initial Accuracy, 10ppm/°C Max Drift</td>
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<td>LTC2400</td>
<td>24-Bit, No Latency ΔΣ ADC in SO-8</td>
<td>0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA</td>
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<td>LTC2410</td>
<td>24-Bit, No Latency ΔΣ ADC with Differential Inputs</td>
<td>0.8µVRMS Noise, 2ppm INL</td>
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<tr>
<td>LTC2411/LTC2411-1</td>
<td>24-Bit, No Latency ΔΣ ADCs with Differential Inputs in MSOP</td>
<td>1.45µVRMS Noise, 4ppm INL, Simultaneous 50Hz/60Hz Rejection (LTC2411-1)</td>
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<td>LTC2413</td>
<td>24-Bit, No Latency ΔΣ ADC with Differential Inputs</td>
<td>Simultaneous 50Hz/60Hz Rejection, 800nVRMS Noise</td>
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<td>LTC2415/LTC2415-1</td>
<td>24-Bit, No Latency ΔΣ ADCs with 15Hz Output Rate</td>
<td>Pin Compatible with the LTC2410</td>
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<tr>
<td>LTC2414/LTC2418</td>
<td>8-/16-Channel 24-Bit, No Latency ΔΣ ADCs</td>
<td>0.2ppm Noise, 2ppm INL, 3ppm Total Unadjusted Errors 200µA</td>
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<td>LTC2440</td>
<td>High Speed, Low Noise 24-Bit ΔΣ ADC</td>
<td>3.5kHz Output Rate, 200nV Noise, 24.6 ENOBs</td>
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<td>LTC2480</td>
<td>16-Bit ΔΣ ADC with Easy Drive Inputs, 600nV Noise, Programmable Gain, and Temperature Sensor</td>
<td>Pin Compatible with LTC2482/LTC2484</td>
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<td>16-Bit ΔΣ ADC with Easy Drive Inputs, 600nV Noise, I2C Interface, Programmable Gain, and Temperature Sensor</td>
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<td>LTC2482</td>
<td>16-Bit ΔΣ ADC with Easy Drive Inputs</td>
<td>Pin Compatible with LTC2480/LTC2484</td>
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<td>LTC2483</td>
<td>16-Bit ΔΣ ADC with Easy Drive Inputs, and I2C Interface</td>
<td>Pin Compatible with LTC2481/LTC2485</td>
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<td>LTC2484</td>
<td>24-Bit ΔΣ ADC with Easy Drive Inputs</td>
<td>Pin Compatible with LTC2480/LTC2482</td>
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<tr>
<td>LTC2485</td>
<td>24-Bit ΔΣ ADC with Easy Drive Inputs, I2C Interface, and Temperature Sensor</td>
<td>Pin Compatible with LTC2481/LTC2483</td>
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<td>LTC2496</td>
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